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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TI-24953
Total Pages	42
First Named Inventor or Application Identifier	John Mark Anthony et al.
Express Mail Label No.	EL008142897US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 39] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [*Total Sheets* 3]
4. Oath or Declaration [*Total Pages*]
   - a. [ ] Newly executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* *[Note Box 5 below]*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: unsigned Declaration and... Power of Attorney

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information.*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

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FEE TRANSMITTAL

Note. Effective October 1, 1997.
Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 1,558.00

Complete if Known	
Application Number	
Filing Date	Herewith
First Named Inventor	John Mark Anthony, et al.
Group Art Unit	
Examiner Name	
Attorney Docket Number	TI-24953

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

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Deposit Account Name: Texas Instruments Incorporated

[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

[ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [ ] Payment Enclosed:
[ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790.00
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790.00

2. CLAIMS

			Extra		Fee from below	=	Fee Paid
Total Claims	40	-20 =	20	X	22	=	440
Independent Claims	7	- 3 =	4	X	82	=	328
Multiple Dependent Claims				X		=	-0-

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 768.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) -0-

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	David Denker			Reg. Number	40,987
Signature		Date	1/5/98	Deposit Account User ID	

HIGH PERMITTIVITY SILICATE GATE DIELECTRIC

RELATED PATENT APPLICATIONS

This application claims priority from the following U.S. provisional applications: No. 60/053,661, filed 7/24/97; No. 60/053,616, filed 07/24/97; and No. 60/053,617 filed, 07/24/97.

This invention is related to concurrently filed applications Serial No. TBD (TI-25859) and Serial No. TBD (TI-26146), which are incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates generally to semiconductor device structures and methods for forming such, and more specifically to such structures and methods related to gate dielectrics for field effect devices formed on integrated circuits.

BACKGROUND OF THE INVENTION

Semiconductor devices such as field effect transistors are common in the electronics industry. Such devices may be formed with extremely small dimensions, such that thousands or even millions of these devices may be formed on a single-crystal silicon substrate or "chip" and interconnected to perform useful functions in an integrated circuit such as a microprocessor.

Although transistor design and fabrication is a highly complex undertaking, the general structure and operation of a

transistor are fairly simple. With reference to Fig. 1, a simplified field effect transistor is shown in cross-section. In a field effect transistor a portion of the substrate **100** near the surface is designated as the channel **120** during processing. Channel **120** is electrically connected to source **140** and drain **160**, such that when a voltage difference exists between source **140** and drain **160**, current will tend to flow through channel **120**. The semiconducting characteristics of channel **120** are altered such that its resistivity may be controlled by the voltage applied to gate **190**, a conductive layer overlying channel **120**. Thus by changing the voltage on gate **190**, more or less current can be made to flow through channel **120**. Gate **190** and channel **120** are separated by gate dielectric **180**; the gate dielectric is insulating, such that between gate **190** and channel **120** little or no current flows during operation (although "tunneling" current is observed with thin dielectrics). However, the gate dielectric allows the gate voltage to induce an electric field in channel **120**, giving rise to the name "field effect transistor."

Generally, integrated circuit performance and density may be enhanced by "scaling", that is by decreasing the size of the individual semiconductor devices on a chip. Unfortunately, field effect semiconductor devices produce an output signal that is proportional to the width of the channel, such that scaling

reduces their output. This effect has generally been compensated for by decreasing the thickness of gate dielectric **180**, thus bringing the gate in closer proximity to the channel and enhancing the field effect.

As devices have scaled to smaller and smaller dimensions, the gate dielectric thickness has continued to shrink. Although further scaling of devices is still possible, scaling of the gate dielectric thickness has almost reached its practical limit with the conventional gate dielectric material, silicon dioxide. Further scaling of silicon dioxide gate dielectric thickness will involve a host of problems: extremely thin layers allow for large leakage currents due to direct tunneling through the oxide; because such layers are formed literally from a few layers of atoms, exacting process control is required to repeatably produce such layers; uniformity of coverage is also critical because device parameters may change dramatically based on the presence or absence of even a single monolayer of dielectric material; and finally, such thin layers form poor diffusion barriers to impurities.

Realizing the limitations of silicon dioxide, researchers have searched for alternative dielectric materials which can be formed in a thicker layer than silicon dioxide and yet still produce the same field effect performance. This performance is often expressed as "equivalent oxide thickness": although the alternative material layer may be thick, it has the equivalent

effect of a much thinner layer of silicon dioxide (commonly called simply "oxide"). Many, if not most, of the attractive alternatives for achieving low equivalent oxide thicknesses are metal oxides, such as tantalum pentoxide and barium strontium titanate.

Researchers have found formation of such metal oxides as gate dielectrics to be problematic. At typical metal oxide deposition temperatures, the oxygen ambient or oxygen-containing precursor required to form them tends to also oxidize the silicon substrate, producing an oxide layer at the interface between the substrate and the gate dielectric. The presence of this interfacial oxide layer increases the effective oxide thickness, reducing the effectiveness of the alternative gate dielectric approach. The existence of the interfacial oxide layer places an ultimate constraint on the performance of an alternative dielectric field effect device.

SUMMARY OF THE INVENTION

The present invention comprises a semiconductor device structure utilizing a metal silicate gate dielectric layer, and a method for making the same. With the present invention, a metal silicate gate dielectric may be formed with a dielectric constant substantially higher than that of either conventional thermal silicon dioxide or silicon nitride dielectrics, and thus the metal silicate dielectric layer may be made substantially

thicker than a conventional gate dielectric with equivalent field effect. However, it is believed that the present invention largely avoids disadvantages, such as interfacial silicon dioxide formation and high interface state densities, that are found with conventional alternative dielectrics.

The present invention generally avoids the problems of other alternative dielectrics by employing an oxidized dielectric material comprising a significant amount of silicon, particularly at the silicon/dielectric interface. In one preferred embodiment, a graded silicate layer is formed, such that near the silicon interface the silicate layer has a large SiO_2 component, while the upper portion of the silicate layer has a large metal oxide component. Such a structure employs primarily SiO_2 bonding at the silicon interface, with resulting low interface state densities. However, the high atomic number metal included in the silicate layer can significantly increase the dielectric constant of the film. The present invention also provides for amorphous silicate gate dielectrics, which have dense microstructures and avoid many of the problems associated with grain boundaries in polycrystalline dielectrics.

In one aspect of the invention, a method of fabricating a semiconductor device is disclosed that comprises providing a single-crystal silicon substrate, forming a metal silicate dielectric layer on the substrate, and forming a conductive gate overlying the metal silicate dielectric layer. This method may

comprise one of several methods for forming the metal silicate dielectric layer. For example, a metal may be deposited on a cleaned Si surface, annealed to form a silicide layer, and then oxidized. Or, metal may be deposited on the substrate in an oxidizing ambient, followed by annealing in an oxidizing ambient. Or, metal and silicon may both be deposited on the substrate in a manner otherwise similar to one of the preceding procedures.

In another aspect of the invention, an integrated circuit having a field effect device fabricated thereon is disclosed that comprises a single-crystal silicon semiconducting channel region, a metal silicate gate dielectric overlying this channel region, and a conductive gate overlying this gate dielectric. The gate dielectric may be either an amorphous or a polycrystalline film. The metal silicate may be, for example, zirconium silicate, cerium silicate, zinc silicate, thorium silicate, bismuth silicate, hafnium silicate, lanthanum silicate, tantalum silicate, or a combination of these materials. Preferably, the metal silicate layer has a graded composition comprising a relatively greater ratio of silicon to metal near the semiconducting channel region, as compared to the ratio of silicon to metal near the conductive gate.

BRIEF DESCRIPTION OF THE DRAWINGS

This invention, including the features and advantages thereof, can be best understood by reference to the following drawings, wherein:

Fig. 1 is a cross-sectional view of a typical prior art integrated circuit field effect transistor;

Figs. 2-5 are cross-sectional views of several semiconductor devices, illustrating different surfaces appropriate for deposition of a silicate gate dielectric according to the invention;

Figs. 6-9 are cross-sectional views of a semiconductor device during fabrication according to one preferred embodiment of the invention;

Figs. 10-12 are cross-sectional views of a semiconductor device during fabrication according to a second preferred embodiment of the invention;

Figs. 13-15 are cross-sectional views of a semiconductor device during fabrication according to a third preferred embodiment of the invention; and

Figs. 16-18 are cross-sectional views of a semiconductor device during fabrication according to a fourth preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the invention may be fabricated using a representative Si(100) substrate, as described herein. The description of these embodiments begins, as shown if Fig. 2, after formation of an epitaxial layer **22** on substrate **20** and implantation of an active channel region **24** in epitaxial layer **22**, and assumes that a protective or native silicon oxide region **26** (preferably comprising less than 1 nm of oxide) overlies channel **24** in the region of interest. Such a silicon oxide layer may be formed by heating a clean substrate to 600-700°C for approximately 30 seconds, in an oxygen ambient of ~10^{-3} Torr. Processes for reaching this step in fabrication are all well-known in the art, as are various equivalents to which the present invention is applicable. The examples below assume that the channel **24** is formed in epi-layer **22**. However, the invention is equally applicable to gate dielectrics formed directly on substrate **20**, or other relatively pure Si structures. In the descriptions below, layers **20** and **22**, and region **24** will be used interchangeably, except where the context shows a particular item is meant.

The particular embodiment employed for forming a silicate gate dielectric will dictate whether silicon oxide region **26** will be either left in place and used in the formation of the silicate layer, removed such that the underlying silicon may be

used in the formation of the silicate layer, or removed and replaced with a passivation layer designed to inhibit interaction of the substrate in the metal silicate deposition process. The immediately following description relates to the preparation of the substrate for deposition of silicate-forming materials, and is applicable to the specific embodiments presented thereafter. There are two preferred starting surfaces for the invention if silicon oxide region **26** is to be removed. Region **26** may be removed so as to leave either a clean, bare upper surface **28** as shown in Fig. 3, or a hydrogen-terminated surface as shown in Fig. 4. If oxide region **26** is removed, the bare surface is preferred to the hydrogen-terminated surface if chemical reaction of the highly reactive Si surface can be prevented, e.g. by processing in ultrahigh (less than ~10^{-8} Torr) vacuum until a point in the particular process where exposure to oxygen can be tolerated. Otherwise, the bare Si surface should be terminated with a suitable passivant, such as hydrogen, which inhibits reoxidation and yet may be readily removed at an appropriate point in the process.

The method of oxide removal is not believed to be critical to the practice of the invention, as long as a clean, oxide-free surface can be maintained until an overlying deposition is performed. One preferred method of performing removal of oxide **26** is by exposure to wet HF, for example by dipping the substrate in dilute HF for 30 seconds and rinsing in deionized

water. This both removes the native oxide and hydrogen terminates the surface. Another preferred method is by exposure to HF vapor; this provides similar results, but may be used, e.g., in a cluster tool to further prevent reoxidation or contamination of the surface. Either of these approaches may comprise other appropriate stripping chemicals, with HF or a NH_4F solution being preferred as a last step to provide termination.

Several other methods produce a non-terminated surface **28**, as shown in Fig. 3. One such method with particular applicability to cluster-tool practice is Si flux desorption; it has been found that below 10^{-8} Torr and at 780°C, an Si flux of preferably 1.5 Å/sec for about 600 seconds not only removes native oxide, but produces an atomically smooth, stepped surface that may have advantages for ultrathin gate dielectrics. The alternative is simple desorption by heating of the substrate to high temperature in vacuum or in an H_2 ambient; it is believed, however, that the Si-flux method results in a superior surface structure. In any of these methods, if the substrate is not to be kept in ultrahigh vacuum until an overlying deposition is completed, surface **28** may be hydrogen terminated, e.g. by exposure to atomic hydrogen produced by a plasma or hot filament in an H_2 ambient.

Surface **28** may also be passivated with an ultrathin layer, such as a silicon nitride or silicon oxynitride layer, that is

not, strictly speaking, an oxide of silicon. Such layers act as a diffusion barrier and provide oxidation resistance to the substrate during formation of the overlying silicate layer. If an oxynitride layer is used, the preferred method of oxynitridation is by exposure to NO. Oxynitrides produced by other methods are not believed to provide sufficient oxidation resistance at the required thicknesses to complete some of the gate dielectric structures disclosed herein, and/or require higher process temperatures, and as such are not preferred. For instance, N_2O processes result in a much smaller incorporation of N than NO processes. NH_3 processes require a pre-existing SiO_2 film, and thus a uniform sub-nanometer oxynitride film appears to be difficult to achieve using NH_3. Additionally, NH_3 annealing apparently incorporates undesirable hydrogen into the film structure.

A typical NO process applicable to the present invention is as follows. The substrate is cleaned to remove the pad oxide. As a final step in the cleaning, the substrate is dipped in dilute HF for 30 seconds, and rinsed in deionized water. The substrate is then placed in a reaction chamber, which is then evacuated to 3×10^{-8} Torr, and then the substrate is heated to 500°C to remove the hydrogen passivation from the substrate surface. The substrate is heated to 700°C, and NO at 4 Torr is introduced into the chamber for 10 seconds to form the oxynitride passivation layer. Fig. 5 depicts a passivation

layer **30**, e.g., either an oxynitride or a nitride passivation layer.

Once the substrate has been prepared to provide either a clean Si surface, an oxide layer, or a protective barrier layer as described above, a metal silicate gate dielectric is formed on the substrate by one of several methods. Although the specific embodiments for gate dielectric formation described below may be readily adapted to the deposition of a wide range of metal silicate compositions and structures, the preferred metal silicate compositions and structures contain several properties as described below.

First, the metal silicate is preferably stable next to silicon. Appropriate silicates generally have a heat of formation that is more negative than the heat of formation of silicon dioxide, as this is believed to form a more stable gate structure and avoid the preferential formation of interfacial silicon dioxide. Some examples of these silicates are those of Ba, La, Hf, and the rare earth elements. Silicates with heat of formations close to that of SiO_2 (e.g. silicates of Sr, Y, Zr, Ta) may also be useful in the present invention, although stability of these silicates is generally less than that of silicates of the first group. Table 1 lists several candidates for this layer in order of heat of formation, with silicon dioxide included for comparison purposes.

Table 1

Material	Heat of Formation (kcal/g/atom of O)
Ca_3SiO_5	-138
Ca_2SiO_4	-135
Ba_2SiO_4	-124
$CaSiO_3$	-123
$SrSiO_3$	-123
Mg_2SiO_4	-122
Na_2SiO_3	-121
$BaSiO_3$	-120
$MgSiO_3$	-119
$ZrSiO_4$	-115
$CeSiO_4$	-115
SiO_2	-103

Second, it is preferred that the metal silicate have a high dielectric constant as compared to the dielectric constant of silicon dioxide (~4) or the dielectric constant of silicon nitride (~7). Generally, the dielectric constant of silicates increases with the atomic number of the metal included; higher atomic weight metals such as Ba, La, Hf, and the rare earth elements are therefore preferred.

Third, the silicate may be formed as either a polycrystalline or an amorphous film. Generally, polycrystalline films will have better dielectric constant. However, amorphous films generally have higher breakdown performance, form a better diffusion barrier, and have lower interface state densities. Also, with many of the preferred embodiments for formation of a silicate dielectric according to the present invention, formation of an amorphous film may be

easier than formation of a polycrystalline film because of the uniform stoichiometry required for a polycrystalline film. Amorphous silicate films may also be stabilized by the inclusion of more than one metal in a mixed-metal silicate film.

Finally, the present invention comprehends a graded dielectric composition. In a preferred embodiment, a silicate film may be formed where the ratio of silicon to metal varies as a function of depth in the film. For example, a graded silicate film may be formed that is mainly SiO_2 at the substrate interface (e.g. 2-10 mol% metal oxide), thus providing an interface with a quality similar to that obtained with pure SiO_2. The ratio of silicon to metal is decreased with a grading profile that results preferably in a greater percentage of metal oxide near the top of the gate dielectric film.

Embodiment 1

In one embodiment according to the invention, a metal silicate gate dielectric is formed by depositing metal on a clean Si surface, annealing this structure to form a metal silicide, oxidizing the silicide layer, and annealing this structure. In this embodiment, a substrate such as shown in either Fig. 3 or Fig. 4 is used. If surface **28** is passivated as shown in Fig. 4, the substrate can be briefly heated to above 500°C in vacuum or an inert ambient to remove the passivation.

Referring to Fig. 6, a metal layer **32** (e.g. zirconium or hafnium) is deposited directly on surface **28**, e.g. by sputtering, evaporation, chemical vapor deposition (CVD) or plasma CVD. Sputter deposition is preferably done with a low-energy plasma system, such as collimated or long-throw sputtering; it should be noted that low deposition rates (e.g. on the order of a few angstroms per second) are preferred, as the total thickness to be deposited is small and uniformity is desired. For an 8" wafer, deposition may be completed in a system with a base pressure of ~10^{-8} Torr, an operating pressure of ~10^{-4} Torr, and a separation between the sputter gun and the wafer of 16 inches, and the wafer may be rotated to improve uniformity. Ar is an acceptable sputter gas, and the wafer may be maintained at a temperature of 400°C during deposition.

As an alternative to sputtering, metal layer **32** may be deposited by evaporation from an e-beam source onto a substrate at 500°C, with a net deposition rate on the order of tenths of angstroms to a few angstroms per second. The substrate is preferably rotated to improve uniformity. Other alternative methods include CVD or plasma CVD using appropriate precursors, such as zirconium tetrachloride and hydrogen gas. Again, with these methods low deposition rates and temperatures (600°C and lower) are preferred, and a downstream plasma type reactor is preferred to a reactor where the plasma is generated at the substrate.

Referring to Fig. 7, a metal silicide layer **34** is formed by annealing substrate **20** with metal layer **32** in an inert ambient, a reducing ambient, or vacuum. Although exact values will depend on the metal selected and the thickness of silicide desired, a 20 second anneal at 700°C in vacuum will generally suffice. During most silicide processes, silicon from substrate **20** diffuses into metal layer **32** to form metal silicide layer **34**. It should be noted that with this technique, an excessively thick metal layer **32** may be deposited, such that less than the entire layer **32** is converted to silicide during the anneal. In this case, the thickness of the silicide is controlled by the anneal time, and the excess metal is etched away after the silicide anneal step.

Referring now to Fig. 8, silicide layer **34** is converted to a silicate layer **36** by oxidation. Control of oxidation is critical during this step, as under-oxidation will result in decreased resistivity and over-oxidation may result in decreased capacitance for layer **36** (due to oxidation of the underlying silicon). Many oxygen anneal processes are available for this step, such as a low temperature O_2 anneal with or without ultraviolet exposure, or an activated oxygen anneal such as O_3, O_3 with ultraviolet exposure, a downstream O_2 plasma, N_2O, or a low temperature O_2 plasma with a DC-biased substrate. As an example of this last process, a downstream 1500W ECR source

operating at 1 mTorr, coupled with ~60V DC and 13.56 MHz or 300 kHz RF applied to the substrate may be used while He backside cooling at 80°C is also applied to the substrate. Processing time is determined experimentally such that both resistivity and dielectric constant lie within an acceptable range.

Generally, a high temperature anneal of silicate layer **36** is selected to densify or crystallize the film after low temperature oxidation. For example, the substrate may be densified by annealing in Ar for 20 seconds at 750°C. This anneal may be done in either an inert or a reducing environment, with a reducing environment particularly useful where metal layer **32** was deposited by CVD using halogens. If a reducing environment is used, an additional low-temperature post-anneal in oxygen may be used to improve dielectric properties of silicate layer **36**.

Finally, with reference to Fig. 9, conductive gate **38** is deposited over silicate gate dielectric **36**. Processes for depositing gate **38** are well known in the art; gate **38** may be formed, by way of example, of doped polysilicon, metal, or a conductive metal oxide. As a variation on this embodiment, the silicide and oxidation steps may be combined, either by introducing an oxidizing ambient before the silicide is completely formed, or by completely overlapping the two steps. In this latter variation, a substrate such as that depicted in

Fig. 2 is preferable, as silicon oxide layer **26** can supply both oxygen and silicon towards the formation of silicate layer **36**.

Embodiment 2

In a second embodiment according to the invention, a metal silicate gate dielectric is formed by depositing metal on a substrate in an oxidizing ambient, followed by annealing. This embodiment preferably utilizes a substrate prepared by one of the methods corresponding to Fig. 2, 3, or 4, and the metal may be deposited by one of the methods described in Embodiment 1, with the following differences.

Referring to Fig. 10, an oxidized metal layer **40** may be deposited on a clean Si surface by sputtering as described above. However, some amount of controlled oxygen activity is used to at least partially oxidize layer **40** as metal is supplied to the substrate. For example, O_2 or H_2O+H_2 may be introduced near the substrate during sputtering with Ar, with an O_2 flow rate of about one-tenth that of the Ar flow rate. For a metal deposition rate of 0.1 nanometers per second, the oxidizing gas is preferably introduced from 0 to 5 seconds after the start of the deposition process.

If oxidized metal layer **40** is produced by the evaporation method, the oxidizer is preferably added near the substrate. To achieve near complete oxidation of the deposited metal, ~5-10 Torr of O_2 may be used for a metal deposition rate of 0.1

nm/sec. If a CVD method is used, appropriate precursors should provide the necessary oxygen (e.g. zirconium tetrachloride and water).

Referring to Fig. 11, layer **40** is reacted with the substrate to form metal silicate layer **36**. Preferably, this is accomplished with a low-temperature oxygen anneal followed by a high temperature anneal, such as those described in the preceding embodiment. One example of a preferred oxygen anneal is a 400°C anneal in O_3 for 60 seconds.

It should be noted that this embodiment may be readily tailored to produce a graded silicate layer. One variation on this method is shown in Fig. 12, wherein layer **40** is deposited over a silicon oxide layer **26**. In such an embodiment, oxygen activity during the anneal may be reduced, and silicate layer **36** may be formed by "stealing" both oxygen and silicon from layer **26**. The grading of the structure may be adjusted by adjusting the relative initial thicknesses of layers **26** and **40**. It may also be appropriate to supply Si to layer **40** by implantation of energetic ions from a remote plasma, using DC bias on the substrate to adjust penetration depth. For example, silane may be used to implant Si into layer **40**.

Embodiment 3

In a third embodiment according to the invention, a metal silicate gate dielectric is formed by depositing both metal and silicon on the substrate in an oxidizing ambient, followed by annealing. In this embodiment, the substrate preparation may be chosen as any of those shown in Figs. 2-5. As this method generally does not rely on silicon from the substrate as a component of the silicate film, a surface that limits oxidation of the substrate, such as the diffusion barrier surface of Fig. 5, is preferred. The metal and silicon may be deposited by one of the methods described in Embodiment 1, with the following differences.

Referring to Fig. 13, an oxidized metal and silicon layer **42** may be deposited on a clean Si surface by sputtering as described in Embodiment 2 for the deposition of oxidized metal layer **40**. The deposition of both metal and silicon is accomplished by replacing the metal target with an appropriate silicide target. The disadvantage of this method is that deposition of a graded layer from a single composition target is difficult.

If oxidized metal and silicon layer **42** is produced by the evaporation method, a method similar to that of Embodiment 2 may be selected. In this case, it is preferred that separate metal and silicon e-beam sources be used such that the ratio of silicon to metal may be varied during deposition.

If a CVD method is used, appropriate precursors should provide the necessary oxygen. Some combinations of precursors, such as a combination of silane, zirconium tetrachloride, and oxygen, may be used to produce uniform stoichiometry layers but may be difficult to use for a graded composition layers. For a graded layer, CVD precursors such as a combination of silicon tetrachloride, zirconium tetrachloride, and water are preferred.

Formation of a high performance silicate layer using this process will generally require both a low-temperature oxygen anneal and a high temperature anneal such as those described in the preceding embodiments. Figs. 14 and 15 depict, respectively, layer **42** deposited on a silicon oxide layer **26** and on a diffusion barrier layer **30** (e.g. a silicon oxynitride layer). As noted, the presence of the diffusion barrier layer **30** allows for the selection of a more aggressive oxygen anneal.

Embodiment 4

In a fourth embodiment according to the invention, a metal silicate dielectric is formed by depositing both metal and silicon on the substrate, followed by annealing. Silicates formed according to this embodiment may be formed on a substrate prepared according to Figs. 2, 3, 4, or 5. In its most straightforward form, this embodiment is a combination of the metal deposition/silicide technique of Embodiment 1 with the

metal/silicon deposition sources of Embodiment 3, such that a silicide is deposited directly.

Referring to Fig. 16, a metal silicide layer **44** may be deposited on a clean Si surface by sputtering as described in Embodiment 1 for the deposition of metal layer **34**. The deposition of both metal and silicon is accomplished by replacing the metal target with an appropriate silicide target. The disadvantage of this method is that deposition of a graded layer from a single composition target is difficult.

If metal silicide layer **44** is produced by the evaporation method, a method similar to that of Embodiment 1 may be selected. In this case, it is preferred that separate metal and silicon e-beam sources be used such that the ratio of silicon to metal may be varied during deposition.

If a CVD method is used, appropriate precursors should provide the necessary oxygen. Some combinations of precursors, such as a combination of silane and zirconium tetrachloride, may be used to produce uniform stoichiometry layers but may be difficult to use for a graded composition layers. For a graded layer, CVD precursors such as a combination of silicon tetrachloride, zirconium tetrachloride, and hydrogen are preferred. Excess hydrogen may be required to prevent the incorporation of chlorine into the film.

Formation of a high performance silicate layer **46** (Fig. 17) from layer **44** using this process will generally require both a

low-temperature oxygen anneal and a high temperature anneal such as those described in the preceding embodiments, particularly Embodiment 1. As noted in the previous embodiment, the presence of a diffusion barrier layer **30** allows for the selection of a more aggressive oxygen anneal.

Embodiment 5

In a fifth embodiment according to the invention, a metal silicate dielectric is formed by depositing both a metal oxide and silicon on the substrate, followed by oxygen annealing. This approach sometimes works better than the silicide approaches above, since the deposited layer is not in a highly reduced (i.e. oxygen deficient) state, at least to the same degree as with the silicide intermediary approaches.

Silicates formed according to this embodiment may be formed on a substrate prepared according to Figs. 2, 3, 4, or 5.

Referring to Fig. 19, a partially reduced metal silicate layer **50** may be deposited on a clean Si surface by co-sputtering a metal oxide, such as ZrO_2 and elemental Si, to form oxygen-deficient zirconium silicate. Alternatively, artisans may co-sputter HfO_2 and Si, to form oxygen-deficient hafnium silicate. Although this zirconium silicate is partially reduced, it may be more readily oxidized to a full silicate than zirconium silicide may be fully oxidized.

For an 8" wafer, deposition may be completed in a system with a base pressure of ~10^{-8} Torr, an operating pressure of ~10^{-3} Torr, and a separation between the sputter gun and the wafer of 16 inches, and the wafer may be rotated to improve uniformity. Ar or a mixture of Ar and O_2 (O_2 ~10-50%) is an acceptable sputter gas, and the wafer may be maintained at a temperature of 400-500°C during deposition. The RF power setting should be low, at about 50-100 watts, to avoid particle and defect formation. The Si power settings are not usually as important, thus they can be set the same as the ZrO_2 settings.

As an alternative to sputtering, a partially reduced metal silicate layer **50** may be deposited by evaporation from separate zirconium oxide and silicon e-beam sources onto a substrate at 500-600°C, with a net deposition rate on the order of tenths of angstroms to a few angstroms per second. The substrate is preferably rotated to improve uniformity.

Referring now to Fig. 8, partially reduced metal silicate layer **50** is converted to a silicate layer **52** by oxidation. Control of oxidation is critical during this step, as under-oxidation will result in decreased resistivity and over-oxidation may result in decreased capacitance for layer **52** (due to oxidation of the underlying silicon). Post-anneals in O_2 at about 400-550° for up to about 30 minutes generally increase capacitance while maintaining low leakage current. Anneals at higher temperatures or longer times tend to degrade capacitance.

Many oxygen anneal processes are available for this step, such as a low temperature O_2 anneal, with or without ultraviolet exposure, or an activated oxygen anneal such as O_3, O_3 with ultraviolet exposure, a downstream O_2 plasma, N_2O, or a low temperature O_2 plasma with a DC-biased substrate. As an approximate example of this last process, a downstream 1500W ECR source operating at 1 mTorr, coupled with ~60V DC and 13.56 MHz or 300 kHz RF applied to the substrate may be used while He backside cooling at 80°C is also applied to the substrate. Processing time is determined experimentally such that both resistivity and dielectric constant lie within an acceptable range.

Generally, a high temperature anneal of silicate layer **52** is selected to densify or crystallize the film after low temperature oxidation. For example, the substrate may be densified by annealing in Ar for **20** seconds at **750°C**. This anneal may be done in either an inert, reducing or an oxidizing environment, with a reducing environment particularly useful where partially reduced metal silicate layer **50** was deposited by CVD using halogens. If a reducing environment is used, an additional low-temperature post-anneal in oxygen may be used to improve dielectric properties of silicate layer **52**. For physical vapor deposited (PVD) dielectrics, an inert or oxidizing ambient is generally preferred. As noted in a

previous embodiment, the presence of a diffusion barrier layer **30** allows for the selection of a more aggressive oxygen anneal. The independent introduction of the metal oxide, such as ZrO_2, and the silicon allows for direct control of a graded metal-to-silicon profile of the silicate dielectric.

We have found that, for gate dielectrics, it is not necessarily desirable to form exactly stoichiometric $ZrSiO_4$. Instead, it is sometimes preferable to form slightly Zr-rich or Zr-deficient films. Stoichiometric $ZrSiO_4$ will crystallize more easily, but non-stoichiometric films remain more stable in amorphous phases. Further, controlling the Zr-content allows control of the dielectric constant, as well as SiO_2-like interface properties. Oxygen-rich silicates seem to exhibit lower leakage currents and better interface properties, because a more SiO_2-like interface and film improves both.

In a variation of this embodiment, it is possible to make slight changes to the oxygen content of the partially reduced metal silicate layer **50**. A slightly higher oxygen content can be obtained by substituting SiO_2 for the Si in either the sputtering or evaporation processes. This SiO_2 sputtering will form SiO, which will thus provide additional oxygen beyond the ZrO_2 and Si, yet not provide enough oxygen to form stoichiometric $ZrSiO_4$.

It is often desirable to form an only slightly reduced metal silicate layer. However, sometimes, it may be preferable

to initially form a more reduced, but not fully reduced metal silicate layer **50**. In these instances, the ZrO_2 can be replaced with Zr, while the Si is replaced by SiO_2. The resulting SiO provides the silicate with more oxygen than the silicide methods described above, but less than the ZrO_2/Si method of embodiment **5.**

Embodiment 6

As an alternative to the preceding embodiments, it is recognized that some of the deposition steps described may be repeated to tailor the composition of a silicate layer. With reference to Figs. 17 and 18, for example, layer **46** may form only an intermediate layer. For example, one or more monolayers of either silicon, metal, or a combination may be deposited using the e-beam evaporation method described in Embodiment 4, followed by a short anneal in an oxidizing ambient to produce intermediate layer **46**. This may then be followed by deposition of a second intermediate layer **48** by a similar process, with the same or a different composition. Using this method, oxidized silicon and oxidized metal layers can be interleaved in an alternating fashion prior to a final anneal. Or, graded compositions can be deposited directly.

The present invention is not limited by the specific embodiments described herein. Although a particular substrate and type of device have been described herein for clarity, this invention has application to Si devices generally which modify

the semiconducting characteristics of an active region using the field effect of an overlying conductive region. Various other combinations of the described steps may be used to produce silicate gate dielectrics, and such are intended to fall within the scope of this invention.

WHAT IS CLAIMED IS:

1. A method of fabricating a field-effect device on an integrated circuit, comprising the steps of:

providing a single-crystal silicon substrate;

forming a metal silicate dielectric layer on the substrate; and

forming a conductive gate overlying the metal silicate dielectric layer.

2. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

exposing a clean Si surface on the substrate;

depositing a first metal on the Si surface;

annealing the substrate in an inert ambient, thereby forming a layer of a silicide of the first metal on the substrate;

oxidizing the layer of a silicide of the first metal, thereby forming the metal silicate dielectric layer.

3. The method of claim 2, further comprising oxidizing less than 1 nanometer of the clean Si surface prior to the depositing a first metal step.

4. The method of claim 2, wherein the oxidizing step comprises simultaneous exposure of the layer of a silicide of the first metal to both an oxidizing gas and a reducing gas.

5. The method of claim 4, wherein the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof.

6. The method of claim 4, wherein the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof.

7. The method of claim 4, wherein the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof , and wherein the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof.

8. The method of claim 2, wherein the oxidizing step comprises exposure of the layer of a silicide to an oxygen plasma.

9. The method of claim 8, wherein the oxygen plasma is exposed to ultraviolet radiation.

10. The method of claim 2, further comprising annealing the metal silicate layer in a non-oxidizing environment, thereby densifying the silicate layer.

11. The method of claim 10, wherein the annealing step is carried out at a temperature sufficient to crystallize the silicate layer.

12. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

depositing a first metal on the substrate in an oxidizing ambient, thereby forming an at least partially oxidized layer on the substrate; and

annealing the substrate in an oxidizing ambient.

13. The method of claim 12, wherein the substrate comprises an oxidized silicon surface layer immediately prior to the depositing step.

14. The method of claim 12, wherein the substrate comprises a clean Si surface immediately prior to the depositing step.

15. The method of claim 12, wherein the depositing a first metal step comprises sputtering material from a target of the first metal onto the substrate.

16. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

depositing a first metal and silicon on the substrate in an oxidizing ambient, thereby forming an at least partially oxidized layer on the substrate; and

annealing the substrate in an oxidizing ambient.

17. The method of claim 16, wherein the substrate comprises an oxidized silicon surface layer immediately prior to the depositing step.

18. The method of claim 16, wherein the substrate comprises a clean Si surface immediately prior to the depositing step.

19. The method of claim 16, wherein the depositing a first metal and silicon step comprises simultaneous deposition of a layer comprising both the first metal and silicon.

20. The method of claim 19, wherein the simultaneous deposition comprises sputtering material from a target comprised of the first metal and silicon onto the substrate.

21. The method of claim 19, wherein the simultaneous deposition comprises evaporating the first metal and silicon from a common source.

22. The method of claim 19, wherein the simultaneous deposition comprises evaporating the first metal and silicon from separate sources.

23. The method of claim 22, wherein the evaporation rate of the separate sources are independently varied during the depositing step, thereby forming a metal silicate dielectric layer having a depth-varying ratio of the first metal to silicon.

24. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises the repeated steps of:

evaporating an intermediate layer of material onto the substrate, the material selected from the group consisting of silicon, a first metal, and combinations thereof, the intermediate layer having a thickness less than 1 nanometer; and

annealing the substrate in an oxidizing ambient, thereby at least partially oxidizing the intermediate layer.

25. The method of claim 24, wherein a first set of one or more of the intermediate layers are silicon, and a second set of one or more of the intermediate layers comprise the first metal, the first set of layers and set second set of layers being deposited in alternating fashion.

26. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

exposing a clean Si surface on the substrate; and

depositing a partially reduced metal silicate layer on the Si surface.

27. The method of claim 26, further comprising annealing the partially reduced metal silicate layer substrate in oxygen, thereby forming the metal silicate dielectric layer.

28. The method of claim 27, wherein the depositing a partially reduced metal silicate layer on the Si surface comprises simultaneous physical vapor deposition of a metal oxide and silicon.

29. The method of claim 27, wherein the depositing a partially reduced metal silicate layer on the Si surface comprises simultaneous physical vapor deposition of zirconium oxide and silicon.

30. The method of claim 27, wherein the depositing a partially reduced metal silicate layer on the Si surface comprises simultaneous physical vapor deposition of hafnium oxide and silicon.

31. An integrated circuit having a field effect device fabricated thereon, the field effect device comprising:

a single-crystal silicon semiconducting channel region;

a metal silicate gate dielectric overlying the channel region; and

a conductive gate overlying the gate dielectric.

32. The integrated circuit of claim 31, wherein the gate dielectric is polycrystalline.

33. The integrated circuit of claim 31, wherein the gate dielectric is amorphous.

34. The integrated circuit of claim 31, wherein the metal silicate is selected from the group consisting of zirconium silicate, barium silicate, cerium silicate, zinc silicate, thorium silicate, bismuth silicate, hafnium silicate, lanthanum silicate, tantalum silicate, and combinations thereof.

35. The integrated circuit of claim 31, wherein the metal silicate gate dielectric has a graded composition comprising a relatively greater ratio of silicon to metal near the semiconducting channel region, as compared to the ratio of silicon to metal near the conductive gate.

36. An integrated circuit made by the method of claim 2.

37. An integrated circuit made by the method of claim 12.

38. An integrated circuit made by the method of claim 16.

39. An integrated circuit made by the method of claim 24.

40. An integrated circuit made by the method of claim 28.

HIGH PERMITTIVITY GATE DIELECTRIC

ABSTRACT OF THE INVENTION

A field effect semiconductor device comprising a high permittivity silicate gate dielectric and a method of forming the same are disclosed herein. The device comprises a silicon substrate **20** having a semiconducting channel region **24** formed therein. A metal silicate gate dielectric layer **36** is formed over this substrate, followed by a conductive gate **38**. Silicate layer **36** may be, e.g., hafnium silicate, such that the dielectric constant of the gate dielectric is significantly higher than the dielectric constant of silicon dioxide. However, the silicate gate dielectric may also be designed to have the advantages of silicon dioxide, e.g. high breakdown, low interface state density, and high stability. The present invention includes methods for depositing both amorphous and polycrystalline silicate layers, as well as graded composition silicate layers.

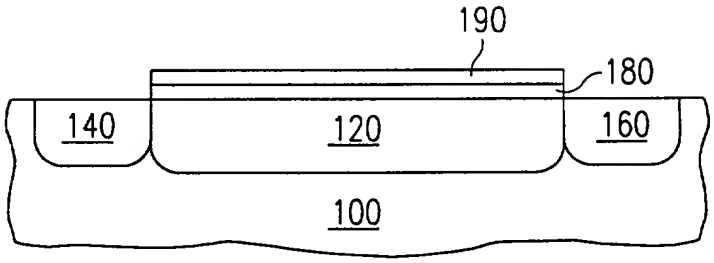

FIG. 1
(PRIOR ART)

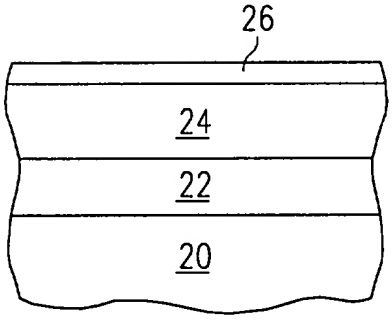

FIG. 2

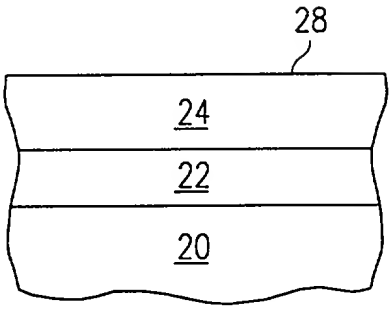

FIG. 3

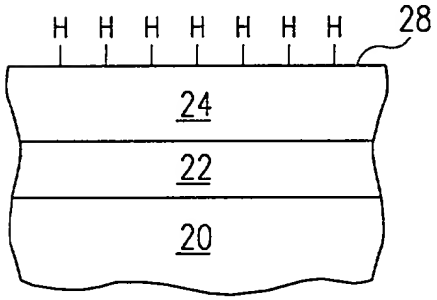

FIG. 4

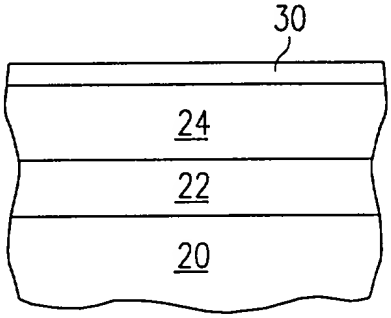

FIG. 5

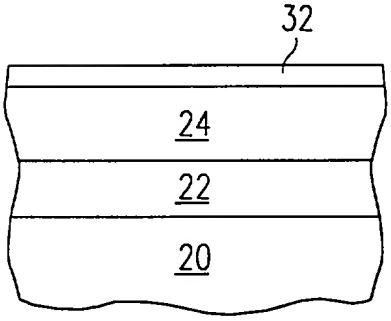

FIG. 6

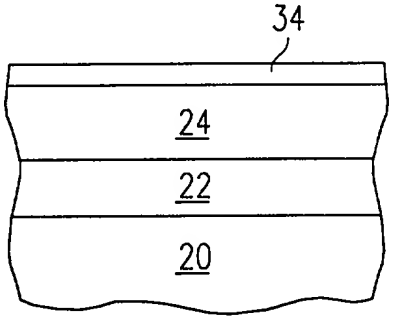

FIG. 7

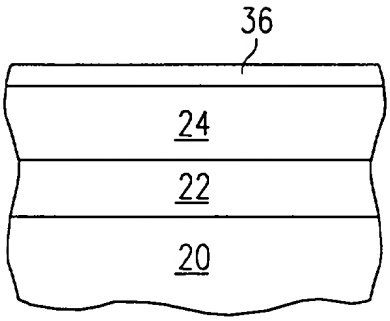

FIG. 8

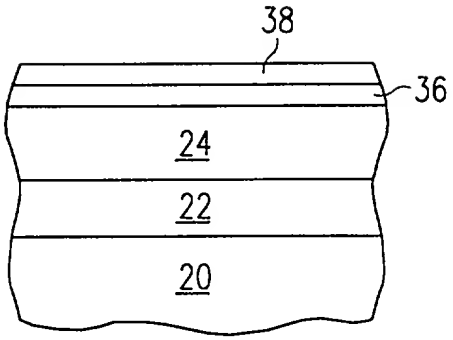

FIG. 9

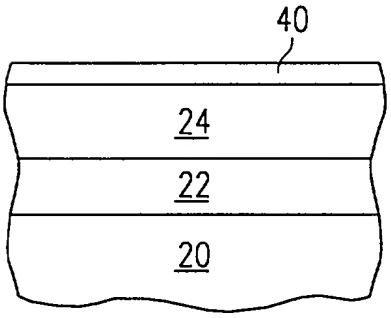

FIG. 10

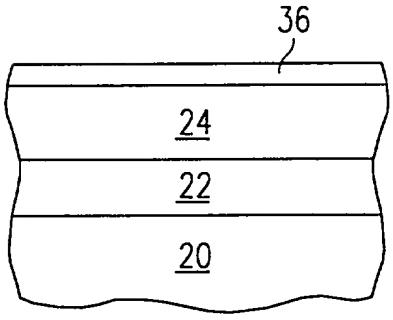

FIG. 11

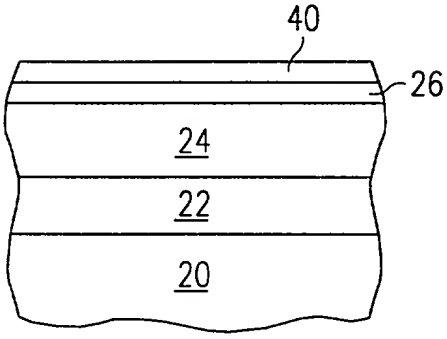

FIG. 12

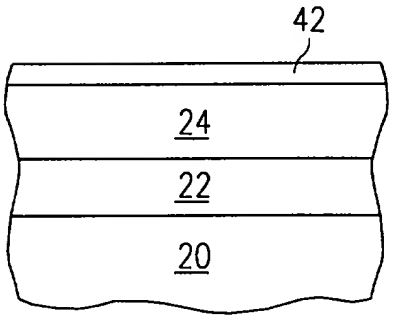

FIG. 13

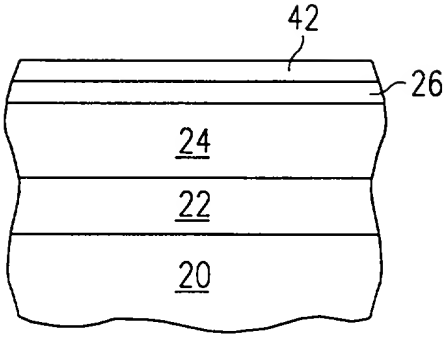

FIG. 14

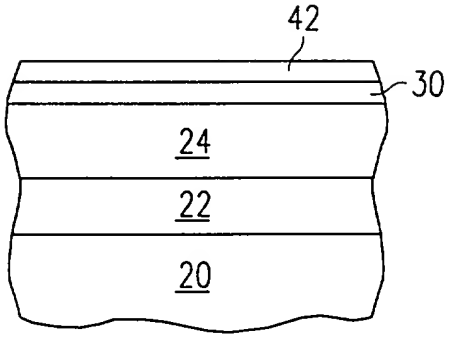

FIG. 15

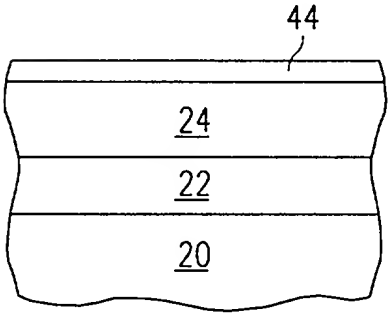

FIG. 16

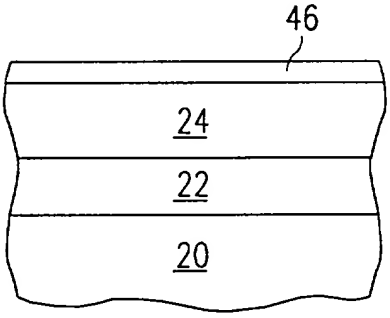

FIG. 17

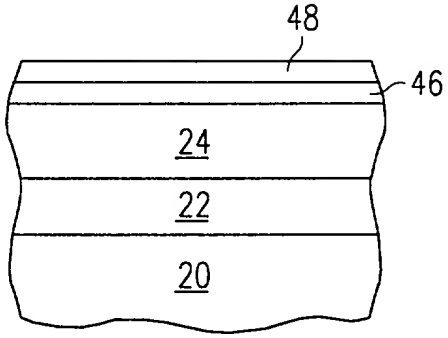

FIG. 18

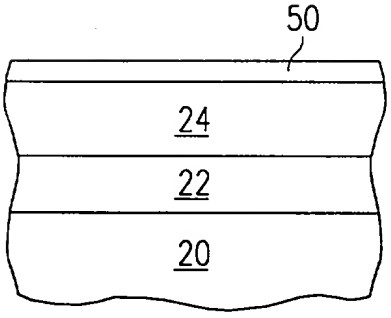

FIG. 19

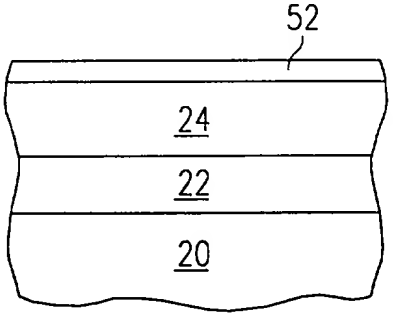

FIG. 20

ATTORNEY'S DOCKET NO.

TI-24953

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, and I believe that I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, dated July, 10, 1998, including the claims.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations 1.56(a).

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States applications listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as denied in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of these provisional applications:

No. 60/053,661, filed 07/24/97; No. 60/053,616, filed 07/24/97; and No. 60/053,617, filed 07/24/97.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

High Permittivity Silicate Gate Dielectric

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

David Denker, Reg. No. 40,987; Richard L. Donaldson, Reg. No. 25,673; William B. Kempler, Reg. No. 28,228; Jay M. Cantor, Reg. No. 19,906; Wade James Brady III, Reg. No. 32,080; Robby T. Holland, Reg. No. 33,304; and Christopher L. Maginniss, Reg. No. 30,288.

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
David Denker Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265	David Denker (972) 917-4388

NAME OF INVENTOR: (1)	NAME OF INVENTOR: (2)	NAME OF INVENTOR: (3)
John Mark Anthony	Scott R. Summerfelt	Robert M. Wallace
RESIDENCE & POST OFFICE ADDRESS: 706 Wood Duck Lane McKinney, TX 75070	RESIDENCE & POST OFFICE ADDRESS: 3202 Bridle Path Ct. Garland, TX 75044	RESIDENCE & POST OFFICE ADDRESS: 428 Park Bend Drive Richardson, TX 75081
COUNTRY OF CITIZENSHIP: USA	COUNTRY OF CITIZENSHIP: USA	COUNTRY OF CITIZENSHIP: USA
SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE:	DATE:	DATE:

ATTORNEY'S DOCKET NO.
TI-24953

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, and I believe that I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, dated July, 10, 1998, including the claims.

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I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States applications listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as denied in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of these provisional applications:

No. 60/053,661, filed 07/24/97; No. 60/053,616, filed 07/24/97; and No. 60/053,617, filed 07/24/97.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

High Permittivity Silicate Gate Dielectric

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

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DATE:	DATE:	DATE: